

**2007 IEEE Region 5 Conference**  
**April 20-22, 2007**  
**University of Arkansas Conference & Continuing Education Center**

**Friday April 20**

**7:00 Registration**  
**CCE Lobby**  
 Pick up badges, Proceedings and Conference handouts

**8:00 Plenary Session**  
**Location: CCE Auditorium**  
**Welcome**  
 Vasundara V. Varadan, Technical Conference Chair  
 Chancellor John White, University of Arkansas – Fayetteville  
 John Meredith, President, IEEE – USA  
 Robert Scolli, IEEE Region 5 Director  
 Edge Nowlin, IEEE Region 5 Conference Chair

**8:15 Plenary Lecture**  
**Dr. Parag Patil, MD, Ph.D**  
**University of Michigan Hospitals, Ann Arbor, MI**  
**Brain – Machine Interfaces – Today and Tomorrow**

Friday April 20, 2007 AM Sessions					
TIME	Session 1	Session 2	Session 3	Session 4	Session 5
9:30-12:45	EM & Biomedical Systems I 410 CCE	Nanostructure Materials and Devices I 409 CCE	Digital Circuits and Systems I 405 CCE	RF, Microwave and Analog Circuits 411 CCE	Control Systems I 402 CCE
12:00-1:30	<b>Lunch</b> (provided to all registered participants)				
Friday April 20, 2007 PM Sessions					
TIME	Session 6	Session 7	Session 8	Session 9	Session 10
1:30 – 4:45	EM & Biomedical Systems I 410 CCE	Nanostructure Materials and Devices II 409 CCE	Digital Circuits and Systems II 405 CCE	Topics in Communications 411 CCE	Power and Energy Systems 402 CCE

**Friday April 20, 2007 Evening**  
**Location: Fayetteville Public Library**  
**405 W. Mountain St.**

**6:30 – 7:30 PM Reception and Poster Session**  
**7:30 – 9:30 PM Dinner**

<b>Saturday April 21, 2007 AM Sessions</b>					
<b>TIM E</b>	<b>Session 11</b>	<b>Session 12</b>	<b>Session 13</b>	<b>Session 14</b>	
8:00-11:50	EM & Biomedical Systems III 410 CCE	Control Systems II 409 CCE	Digital Circuits and Systems III 411 CCE	Radio Frequency Identification 304 CCE	
12:00-1:30	<b>Lunch</b> (provided to all registered participants)				

**Workshop: Saturday, April 21, 2007, 11:30 – 1:45 PM**

**Asynchronous Circuits**

**Presenters:**

Scott C. Smith, Jia Di, Waleed K. Al-Assadi

**Topics to be covered:**

- 1) Introduction to Asynchronous Logic
- 2) Introduction to NULL Convention Logic (NCL)

3) Transistor-Level NCL Gate Design

**Break:** 12:30 – 12:45 (box lunch provided to registered participants)

4) NCL Combinational Circuit Design

5) NCL Throughput Optimizations

6) Low-Power NCL Techniques

7) Testing NCL Circuits

**Laboratory and Research Center Tours: April 21, 2007, Saturday 2:00 – 4:00 PM**

**RFID Center**

**High Density Electronics**

**Nano-Bio Systems Laboratory**

**Microwave & Optics Laboratory for Imaging & Characterization**

**(others to be added)**

**Tour Guides for the different venues will meet interested participants in the lobby of the CCE at 1:50 PM**